



## 256K x 16 Static RAM

### Features

- **High Speed**
  - 55 ns and 70 ns availability
- **Low voltage range:**
  - CY62147CV18: 1.65V–1.95V
- **Pin Compatible w/ CY62147V18/BV18**
- **Ultra-low active power**
  - Typical Active Current: 0.5 mA @ f = 1 MHz
  - Typical Active Current: 2 mA @ f = f<sub>max</sub> (70 ns speed)
- **Low standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

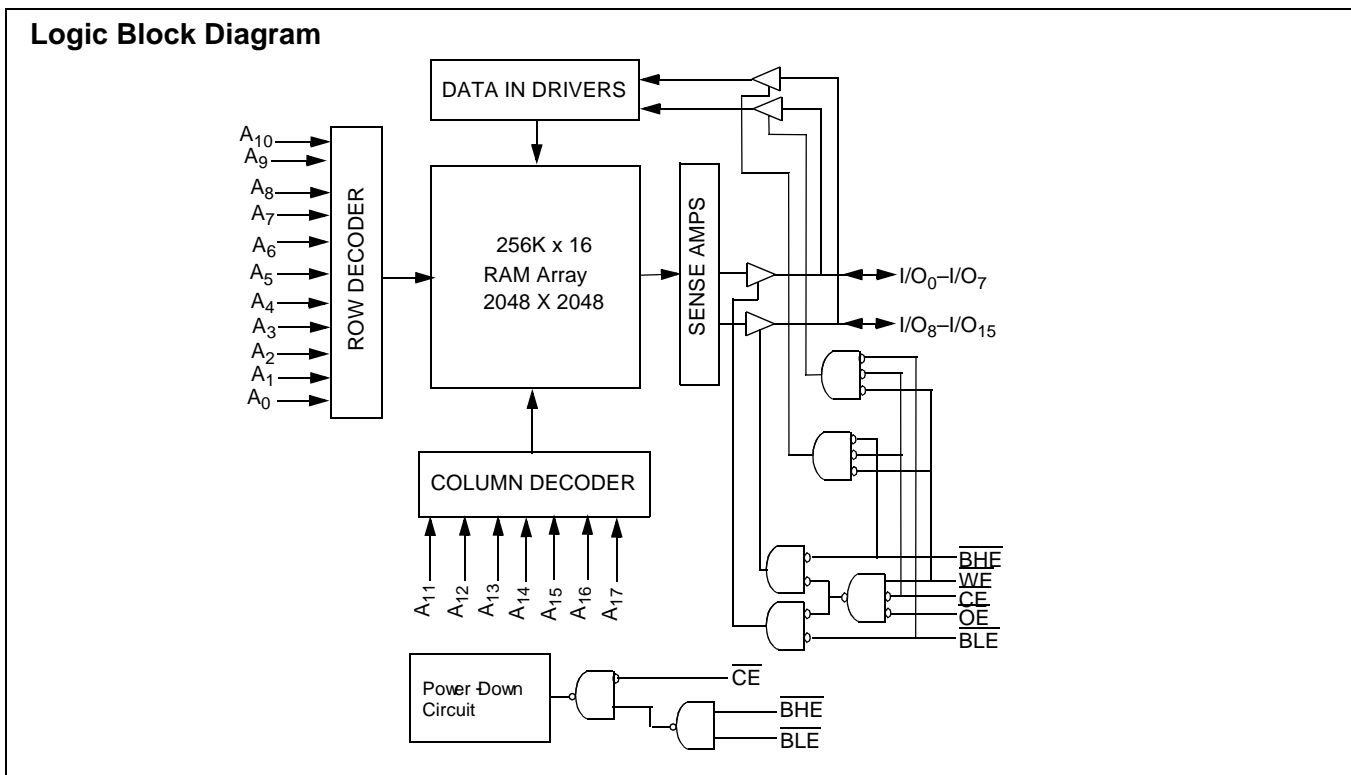
The CY62147CV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces

power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH or both  $\overline{BLE}$  and  $\overline{BHE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

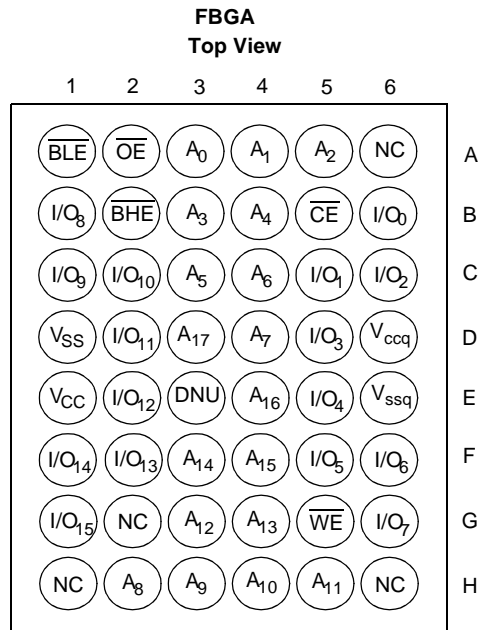
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62147CV18 is available in a 48-ball FBGA package.



MoBL, MoBL2, and More Battery Life are trademarks of Cypress Semiconductor Corporation.

**Pin Configuration<sup>[1, 2]</sup>**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential .....	-0.2V to +2.4V

DC Voltage Applied to Outputs

in High Z State<sup>[3]</sup> ..... -0.2V to  $V_{CC} + 0.2V$

DC Input Voltage<sup>[3]</sup> ..... -0.2V to  $V_{CC} + 0.2V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Device	Range	Ambient Temperature	$V_{CC}$
CY62147CV18	Industrial	-40°C to +85°C	1.65V to 1.95V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)					
					Operating (I <sub>CC</sub> )				Standby (I <sub>SB2</sub> )	
	f = 1 MHz		f = f <sub>max</sub>		Typ. <sup>[4]</sup>		Max.			
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[4]</sup>	V <sub>CC(max.)</sub>						Typ. <sup>[4]</sup>	Max.
CY62147CV18	1.65V	1.80V	1.95V	55 ns	0.5 mA	3 mA	2.5 mA	7 mA	1 μA	10 μA
				70 ns	0.5 mA	3 mA	2 mA	6 mA		

**Notes:**

- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or  $V_{SS}$  to ensure proper application.
- $V_{IL}$  (min) = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$  Typ,  $T_A = 25^\circ C$ .

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62147CV18-55			CY62147CV18-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 1.65V	1.4			1.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 1.65V			0.2			0.2	V
V <sub>IH</sub>	Input HIGH Voltage			1.4		V <sub>CC</sub> + 0.2V	1.4		V <sub>CC</sub> + 0.2V	V
V <sub>IL</sub>	Input LOW Voltage			-0.2		0.4	-0.2		0.4	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 1.95V		2.5	7		2	6	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS levels		0.5	3		0.5	3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, and BLE)			1	10		1	10	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = 1.95V$								

**Capacitance<sup>[5]</sup>**

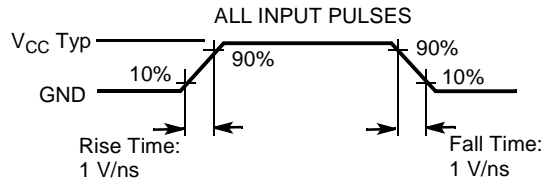
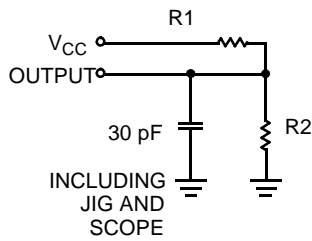
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) <sup>[5]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case) <sup>[5]</sup>		θ <sub>JC</sub>	16	°C/W

**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


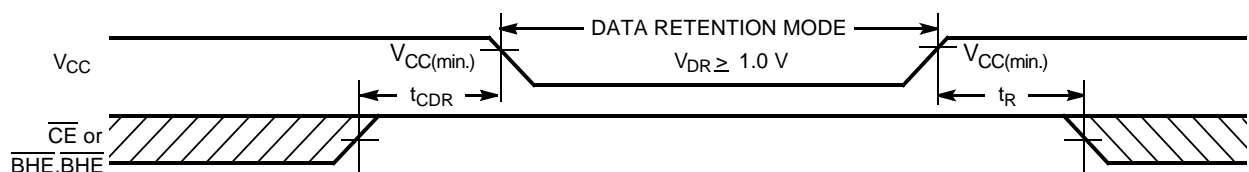
Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8V	UNIT
R1	13500	Ohms
R2	10800	Ohms
R <sub>TH</sub>	6000	Ohms
V <sub>TH</sub>	0.80	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0		1.95	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		1	8	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[6]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform<sup>[7]</sup>**

**Notes:**

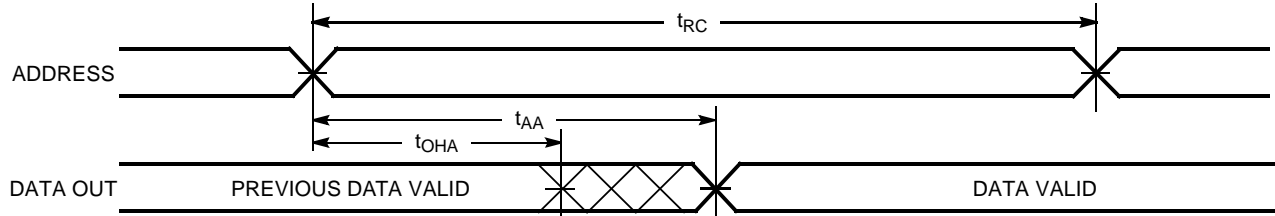
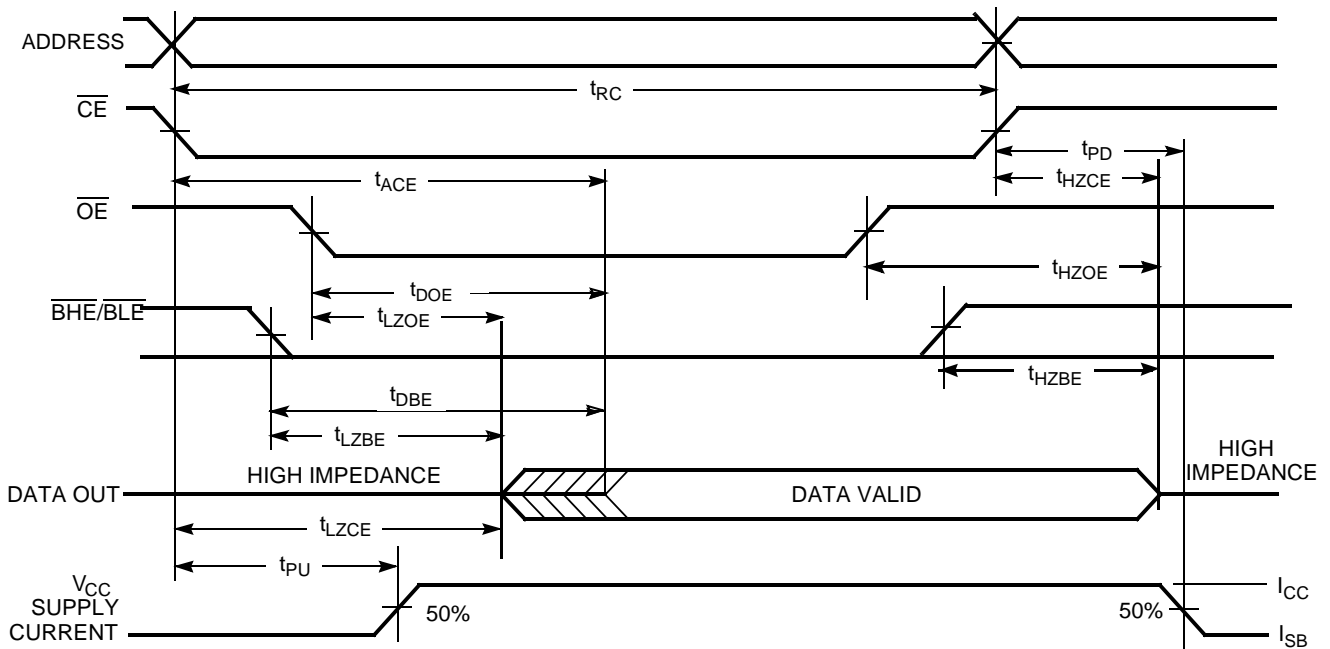
- Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.
- BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

**Switching Characteristics** Over the Operating Range<sup>[8]</sup>

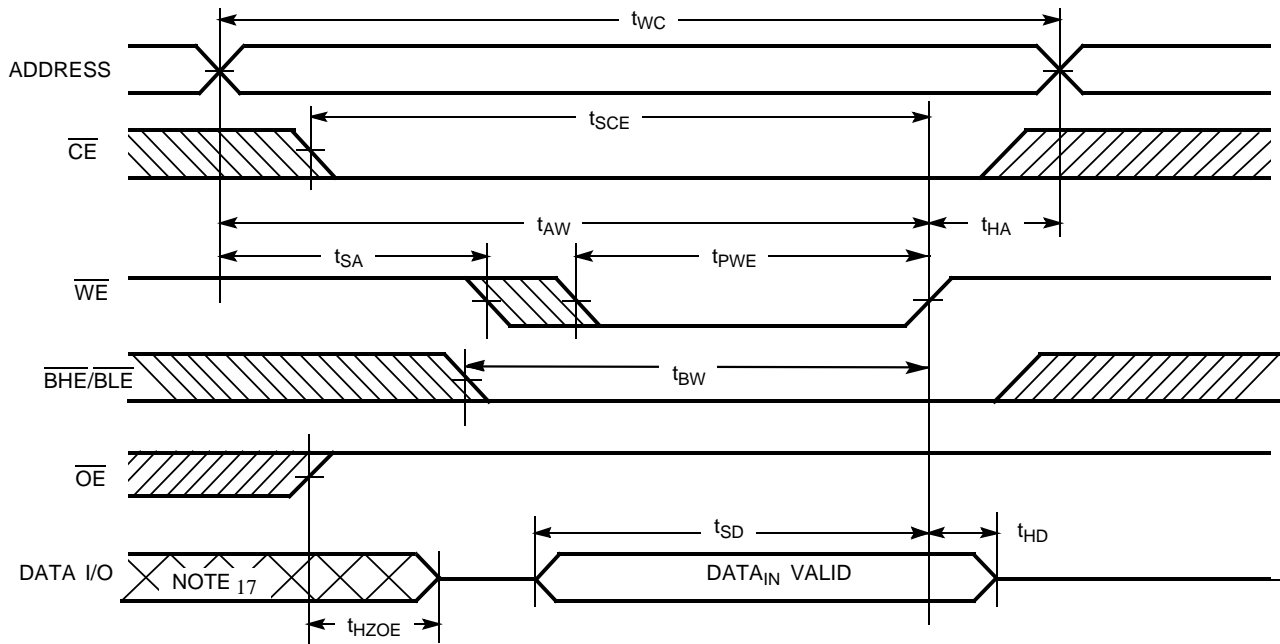
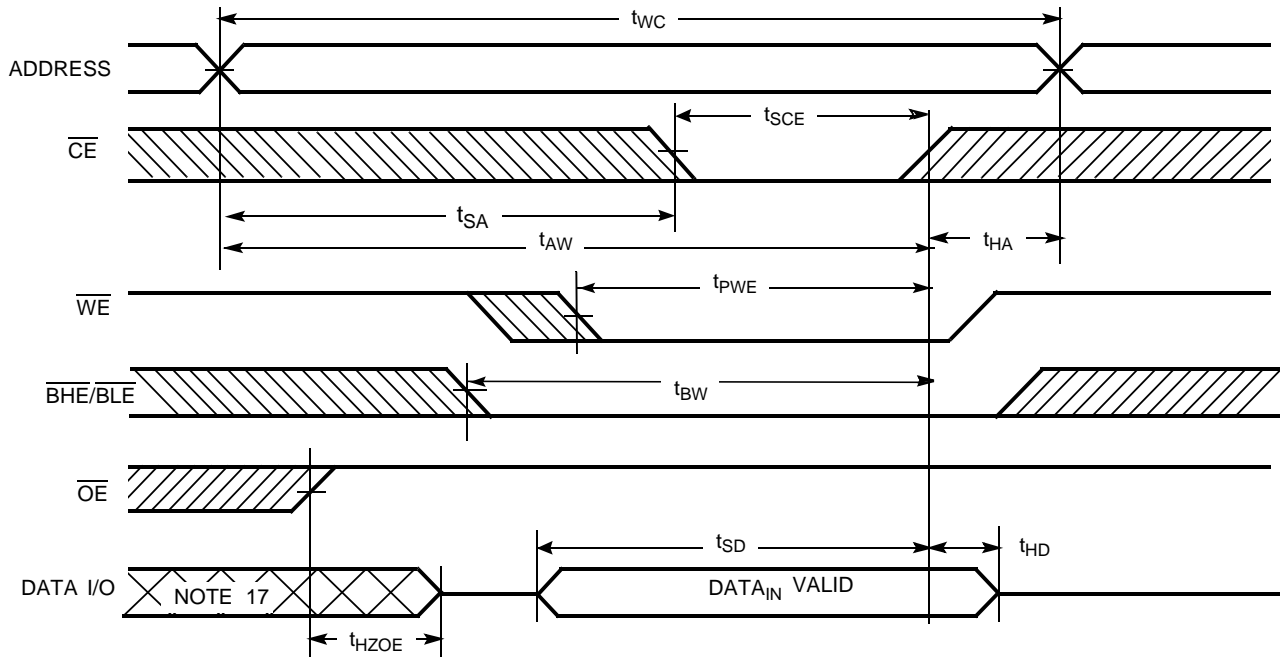
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[9, 10]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	5		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[9]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to High Z <sup>[9, 10]</sup>		20		25	ns
<b>WRITE CYCLE<sup>[11]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	40		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		60		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[9, 10]</sup>		15		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	5		10		ns

**Notes:**

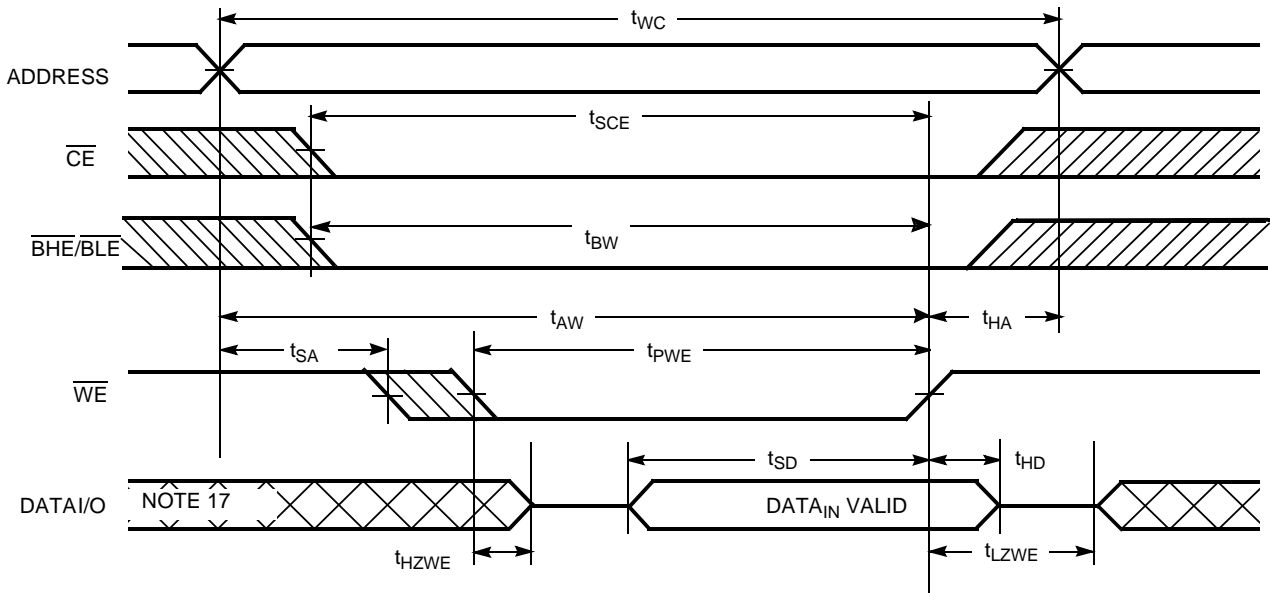
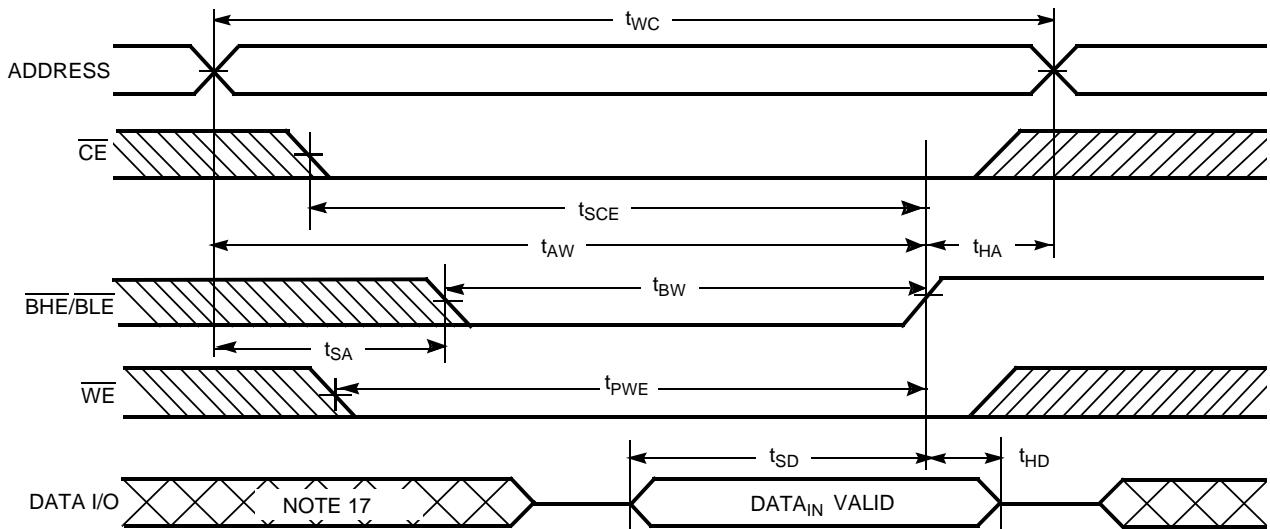
8. Test conditions assume signal transition time of 3ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
9. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
10. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
11. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)** <sup>[12, 13]</sup>

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** <sup>[13, 14]</sup>

**Notes:**

12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , transition LOW.

**Switching Waveforms**
**Write Cycle No. 1 (WE Controlled)**<sup>[11, 15, 16]</sup>

**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)**<sup>[11, 15, 16]</sup>

**Notes:**

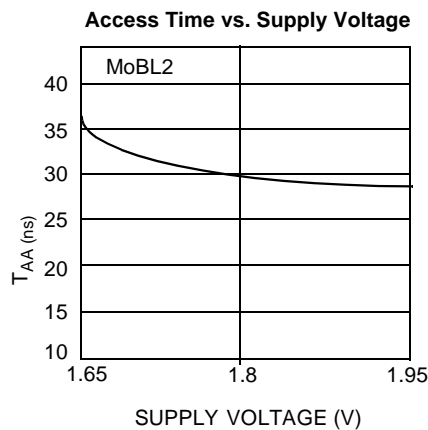
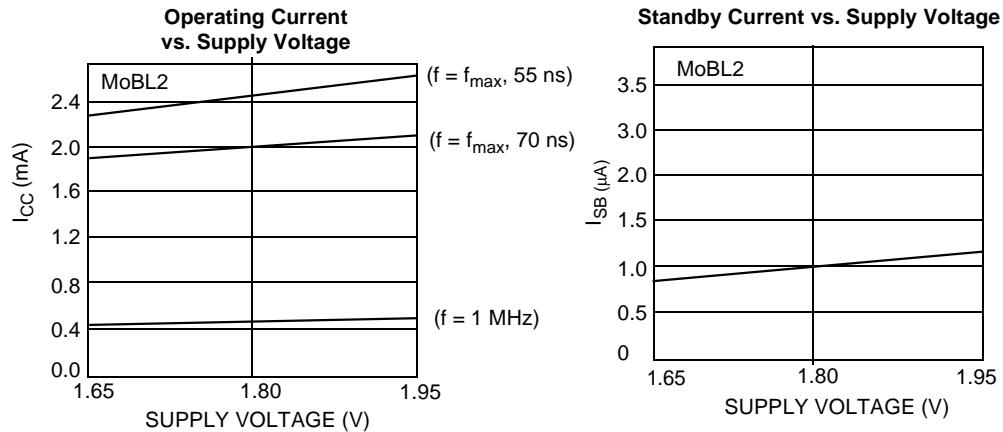
15. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16]</sup>**

**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16]</sup>**




## Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC\ Typ}$ ,  $T_A = 25^\circ\text{C}$ .)

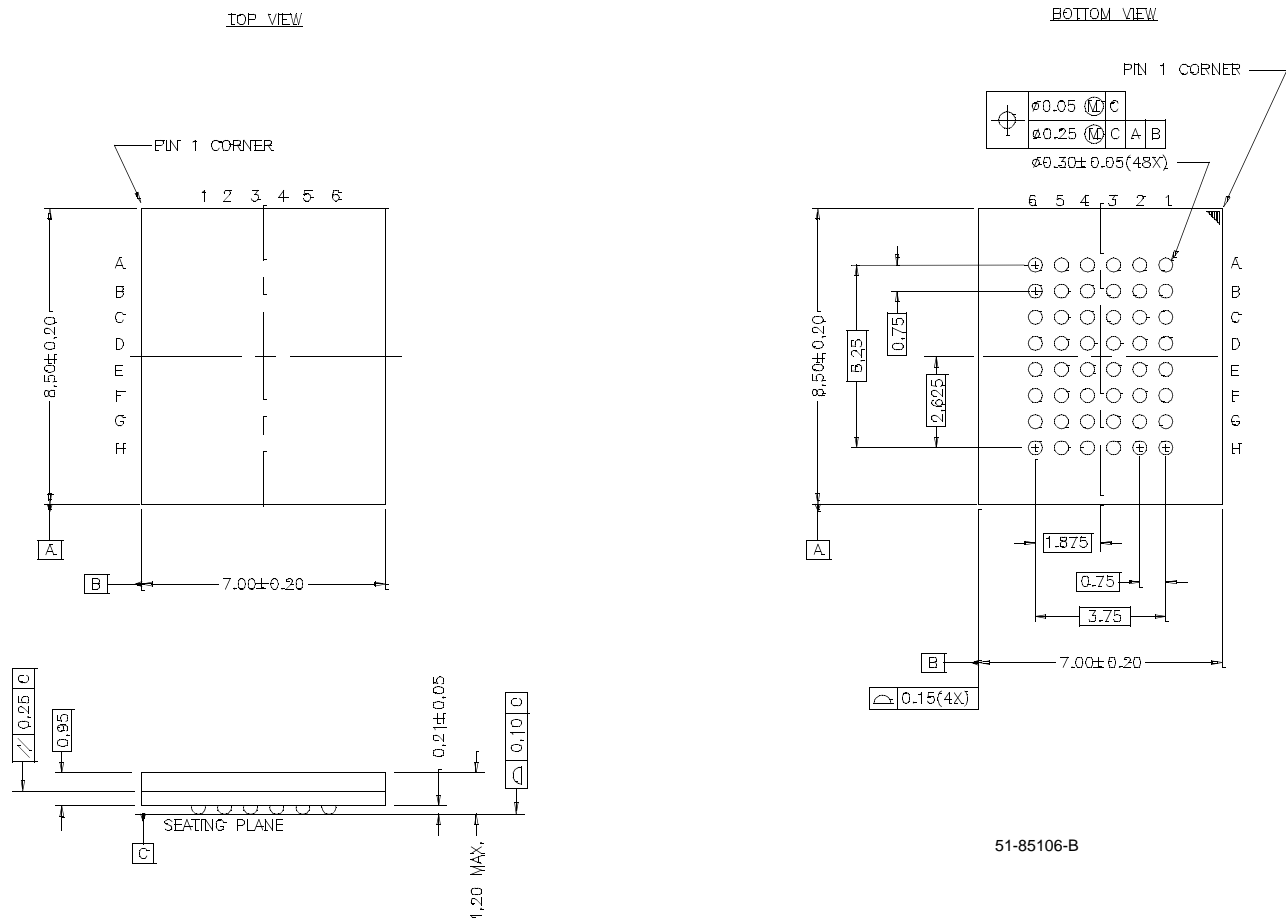


## Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write	Active ( $I_{CC}$ )

**Ordering Information<sup>[18]</sup>**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV18LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62147CV18LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62147CV18LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV18LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

**Package Diagrams**
**48-Ball (7 mm x 8.5 mm x 1.2 mm) Fine Pitch BGA BA48B**

**Note:**

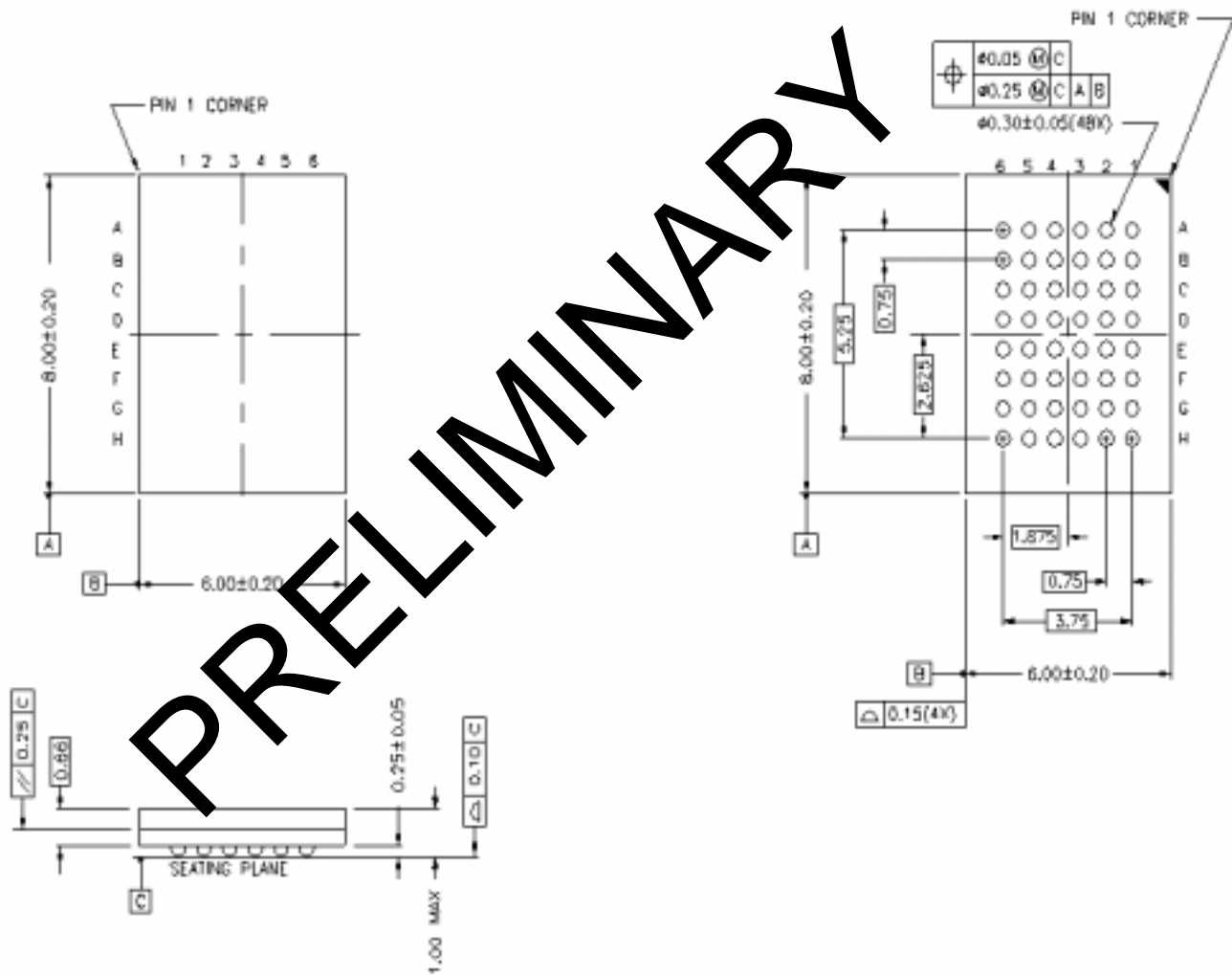
18. Gray Shading represents preliminary information.

Package Diagrams (continued)

48-Ball (6 mm x 8 mm x 1 mm) Fine Pitch BGA BV48A

Top View

Bottom View



PRELIMINARY

Document Title: CY62147CV18 MoBL2™, 256K x 16 Static RAM Document Number: 38-05011				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106265	5/7/01	HRT/MGN	New Data Sheet
*A	108941	08/24/01	MGN	From Preliminary to Final
*B	110573	11/02/01	MGN	Improved $I_{SB}$ Typ. from 1.5 $\mu$ A to 1 $\mu$ A. Improved Typical DC & AC Characteristics graphs. Improved Switching Characteristics: $t_{OHA}$ , $t_{LZCE}$ . Add preliminary package diagram of BV48A. Format standardization